BR FET : A BAND REJECTION FET FOR AMPLIFIER AND MIXER APPLICATIONS

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ABSTRACT

A new type of GaAs FET device, the Band Rejection FET (BR FET), is presented. It is a dual gate FET with a LC series resonant circuit connected in parallel with the intergate ohmic contact that acts as a band rejection filter. The main applications of this device are band rejection amplifiers and image rejection mixers. As an amplifier, the BR FET has a gain of more than 3 dB at 12 ± 0.4 GHz with 20 dB rejection at 9.5 ± 0.4 GHz. As a mixer, the BR FET permits conversion gain (≥ -4 dB) with image frequency rejection of over 30 dB.

Introduction

In SSB receivers, image frequency rejection can be obtained using passive bandpass or bandstop filters or couplers. Under certain conditions, the filter can also be used for image frequency recovery in the mixer[1]. In a GaAs monolithic version of such a receiver, for satellite TV reception for instance, a passive band rejection filter could be used, as proposed in[2], but it would introduce 2 to 3 dB loss at the signal frequency band for an image band rejection of 25 to 30 dB.

In this paper, a solution of the image frequency rejection problem will be proposed using a BR FET, a device that can be used as amplifier or mixer at 12 GHz and that inherently permits the rejection of an undesired frequency band, in our case the image frequency at 9.5 GHz.

The band rejection FET : Technology and characterization

The BR FET is a modified dual gate FET device with inherent rejection of a well defined frequency band. This is obtained by introducing a LC series resonant circuit between the two gates of the FET. The layout is shown in fig. 1 : a 10 µm long intergate ohmic contact is extended to both sides of the epitaxial mesa and ends there on SiO_2 overlay capacitors with a surface of 70 x 70 μm^2 and values of 0.4 to 0.5 pF. Inserting inductances of 0.5 to 0.7 nH between the capacitors and ground creates a series resonance at 9.5 GHz. The signal entering the gate 1 passes through the intergate ohmic contact that short circuits the semiconductor material beneath to it[3] and is trapped at that frequency by the series resonant circuit. The rejection frequency band can be selected independently of tuning of gates 1 and 2 and drain. The inductances are at present realized using small bonding wires but also a on chip integration is envisaged.

The DC behaviour is described using the bidimensional characteristic previously used for dual gate FETs[4] and shown in fig. 2 : it allows determination of internal device voltages (V_{G2D1} and V_{D1S}) of the partial FETs from external applied ones (V_{G2S}, V_{G1S}, V_{DS}). The shaded areas A and M in fig. 2 show the biasing regions for image rejection amplifier (A) and mixer (M) applications of the BR FET.

S parameters of the BR FET between gate 1 and drain have been measured with an automatic network analyzer and are given in Table I. The gate 2 impedance is optimized for maximum S_{21} at 12 GHz.

Considering the values of S_{21} and S_{12}, it is evident that the frequency band 9.2 to 10 GHz is rejected by around 20 dB or more while the 11.6 to 12.4 GHz band remains almost unaffected. The device is therefore predestined for band rejection amplifier or mixer applications.

Freq. (GHz)	S_{11}	φ_{11}	S_{12} (dB)	φ_{12}	S_{21} (dB)	φ_{21}	S_{22}	φ_{22}
8	0.305	-68.9	-21.1	51.9	- 8.4	-39.7	0.649	-87.4
8.6	0.450	-57.2	-25.9	39.1	-12.1	-18.7	0.751	-77.8
9.2	0.546	-52.6	-31.8	3.4	-19.0	-29.4	0.734	-64.2
9.4	0.596	-54.7	-44.8	131.8	-22.8	19.5	0.727	-52.5
9.6	0.592	-54.4	-37.5	85.7	-23.6	25.8	0.759	-39.9
9.8	0.594	-52	-36.8	99.2	-22.8	65.1	0.826	-32.8
10	0.596	-48.4	-35.1	111.8	-19.4	84.7	0.843	-25.6
10.4	0.592	-42.3	-32.9	129.2	-13.2	98.1	0.84	- 7.1
11.0	0.51	-39.9	-27.8	144.7	- 6.2	86.2	0.813	12.6
11.6	0.442	-50.2	-23.9	140.5	- 1.5	56.2	0.778	- 0.5
11.8	0.427	-54.4	-22.9	134.8	- 0.7	41.9	0.823	-29.2
12.0	0.43	-58.3	-22.9	131.1	-0.26	28.3	0.823	-29.2
12.2	0.427	-62.5	-22.9	128	0.0	14.0	0.861	-42.0
12.4	0.422	-66.2	-22.9	125	0.1	0	0.891	-56.0

Table I : S - parameters of BR FET (V_{DS} = 5 V, I_D = 13 mA).

Band rejection amplifier with BR FET

The conception of a band rejection amplifier can easily be made starting with the S parameters of Table I. Using high pass matching circuits at the input and output ports in order to minimize contributions from lower frequencies, the circuit was optimized by means of a network analysis program for maximum gain at 12 ± 0.4 GHz and maximum rejection at 9.5 ± 0.4 GHz. The results are given in fig. 3. The particular configuration of matching elements has been chosen in order to enable bias supplying by the parallel inductances and DC block capacitors ; the circuit optimization was restricted in order to obtain L and C values realizable monolithically by loop inductors and interdigital capacitors. The first realization on 0.63 mm thick Al_2O_3 substrate is shown in fig. 4. $\lambda/4$ open microstrip lines at 9.5 GHz present virtual shorts for the bonding wires connected to the intergate capacitors.

The measured and calculated transmission gain of the BR amplifier is shown in fig. 5. The input and output VSWR are less than 2 and 3 resp. in the passband of 11.6 to 12.4 GHz.

Single-side band noise figure has been measured with an external mixer using a 0.8 to 1.6 GHz I.F. receiver and a 10.7 GHz local oscillator. Best performance was achieved using a metallic disc tuned circuit and is shown in fig. 6 : 6.7 dB noise

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figure were obtained over 700 MHz bandwidth.

Image rejection mixer with BR FET

Dual gate FET mixers offer the possibility to combine signal and local oscillator powers without using cumbersome microstrip couplers which are difficult to integrate. The local oscillator normally enters gate 2 and the signal gate 1 [5]. In that case, mixing is obtained by the nonlinearities of FET 1 for $V_{G2S} \simeq 0$ V (point F1 in fig. 2) and by the nonlinearities of FET 1 and 2 for $V_{G2S} \leq -1.5$ V (point F1,2 in fig. 2). In both cases, the image frequency is mixed down "before" FET 2 and does not "see" the band rejection filter.

For an efficient image rejection therefore mixing has to be effectuated only by the nonlinearities of FET 2, as illustrated in fig. 7. In order to obtain that aim, the BR FET has to be biased into region M (mixer) of its DC characteristic (fig. 2). Mixing occurs here due to switching of FET 2 between saturation and nonsaturation operation by the local oscillator signal V_{G2S} applied on gate 2 and consequent modulation of its channel resistance and transconductance. The first part of the BR FET i.e. FET 1, now acts as a RF preamplifier. The results of image rejection mixing operation of the BR FET are given in fig. 8. Matching has been obtained using metallic discs on gate 1 and 2 while the I.F. was matched at the drain using a double stub tuner, unfortunately increasing the oscillation tendency and limiting the bandwidth of the circuit to about 100 MHz.

An image rejection of over 30 dB compared with the transmitted signal is obtained that partly stems from the image filter ($\simeq$ 20 dB) and partly from input mismatch at the image frequency ($\simeq$10 dB). The SSB noise figure is relatively high since the circuit was matched primarily for high conversion gain and because of the detrimentally high device current necessary in order to operate in region M (fig. 2). Image frequency recovery is also obtained by the image filter since it presents a short circuit directly in front of the mixing FET [1].

Conclusion

The BR FET is a GaAs FET device with 20 dB inherent rejection of a 0.8 GHz wide frequency band. Its operation as image frequency rejection amplifier with 4 dB gain and 7.2 dB noise figure at 12 $\pm$ 0.4 GHz and 20 dB rejection at 9.5 $\pm$ 0.4 GHz has been demonstrated. Employed as a mixer, the BR FET offers conversion gain (4 - 6 dB) and image frequency rejection of more than 30 dB. The device is easily monolithically integrable.

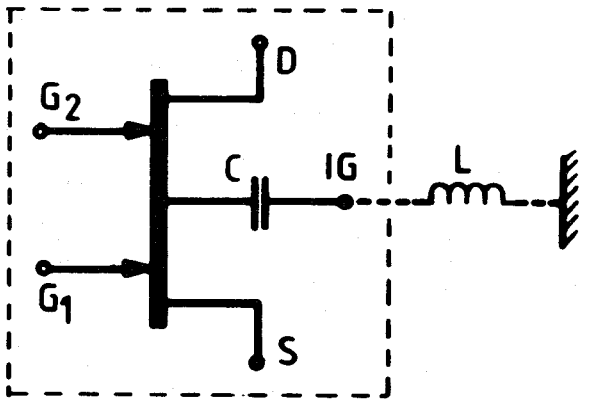

Fig. 1b : Symbol of BR FET

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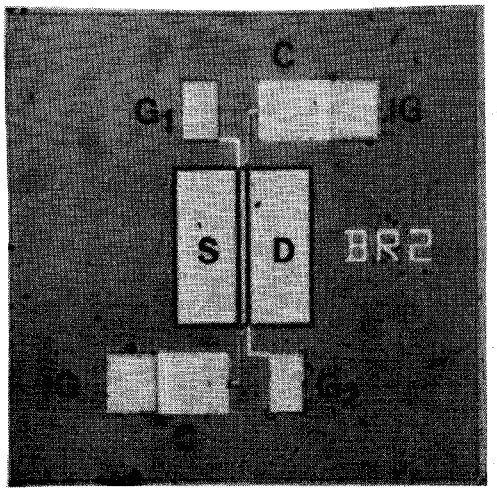

Fig.1a : Layout of BR FET. Chip size is 0.4x0.4 mm^2

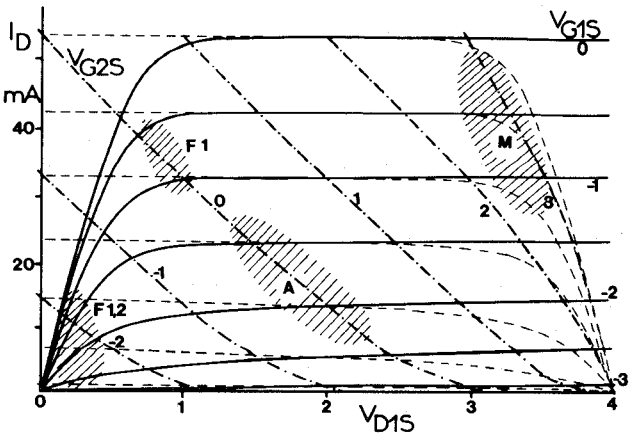

Fig. 2 : Bidimensional DC transfer characteristic of BR FET.

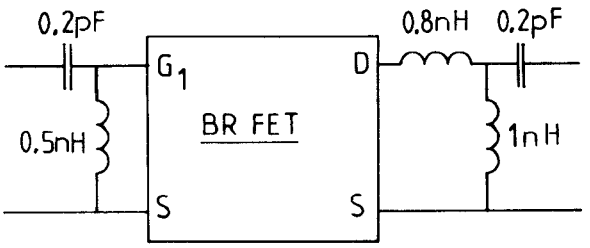

Fig. 3 : Optimized circuit for band rejection amplifier with BR FET.

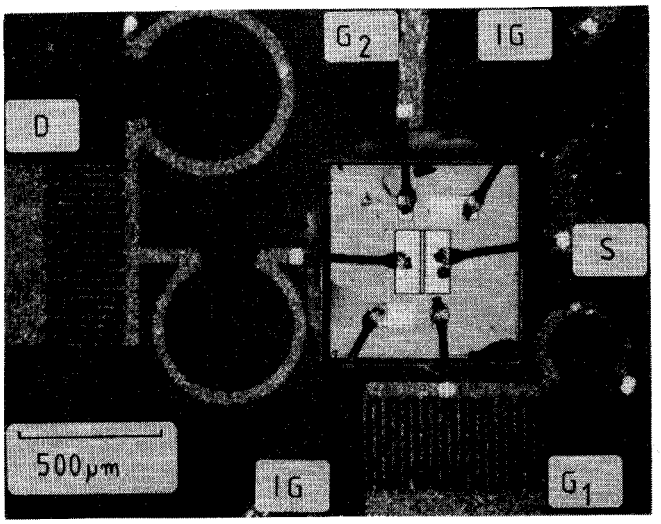

Fig. 4 : Realization of BR FET amplifier on Al_2O_3 using lumped elements.

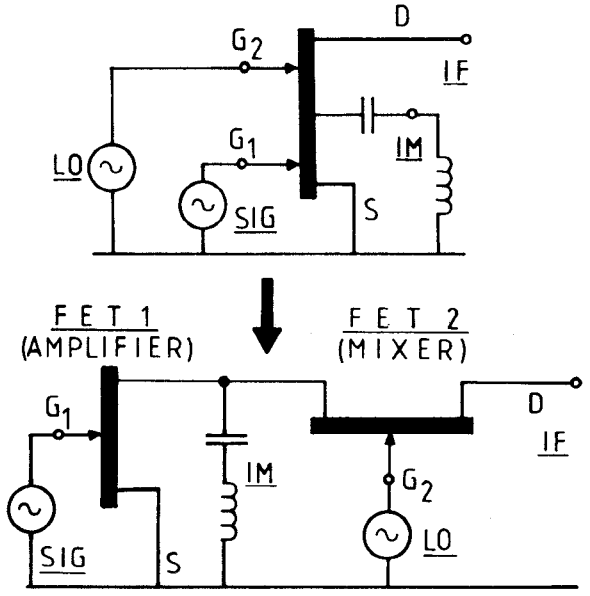

Fig. 7 : Function of BR FET as image rejection mixer

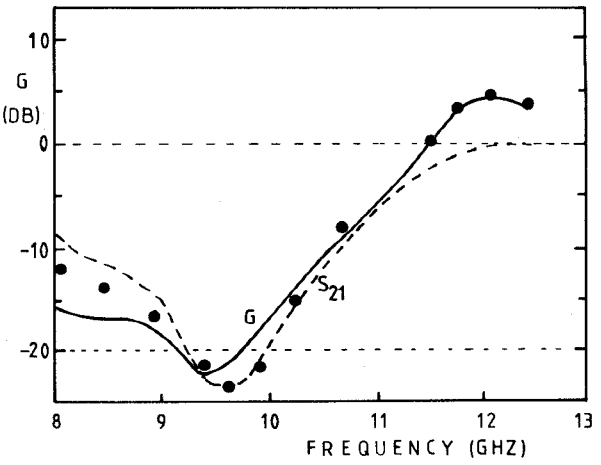

Fig. 5: Calculated (——) and measured (●) gain and S_{21} (---) of BR FET and BR amplifier

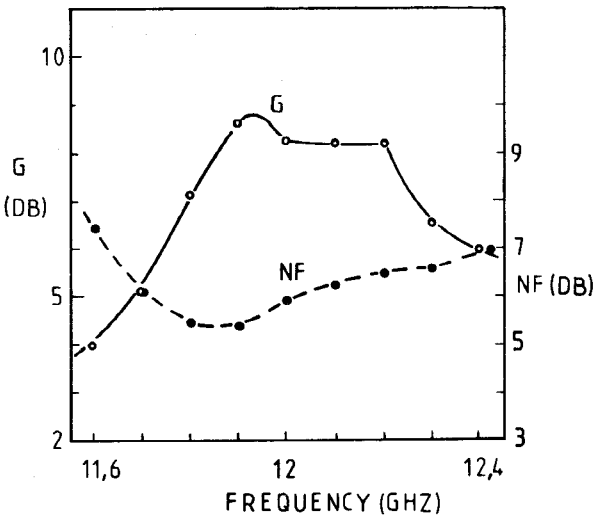

Fig. 6 : Gain and noise figure of disc tuned BR FET amplifier

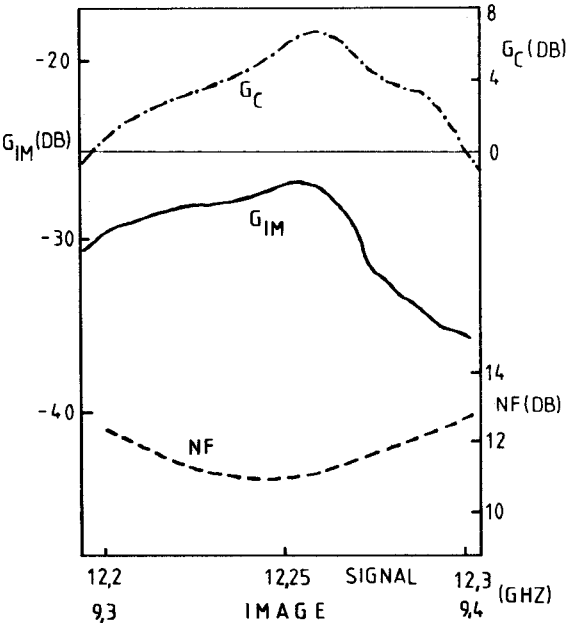

Fig.8 : Performance of BRFET image rejection mixer